first portion of [the] a clock cycle, and for outputting, from said second plurality of shift registers through said multiplexer, the second portion of the reference-chip-sequence signal during a second portion of the clock cycle;

a plurality of data-shift registers, coupled to said spread-spectrum receiver, for shifting a plurality of input-data samples of the received-spread-spectrum signal at [the] a clock rate;

a plurality of exclusive-OR (XOR) gates, coupled to said plurality of data-shift registers and through said multiplexer to said first plurality of shift registers and through said multiplexer to said second plurality of shift registers, responsive to said multiplexer selecting the first plurality of shift registers during the first portion of the clock cycle, for multiplying the first portion of the reference-chip-sequence signal by the plurality of input-data samples during the first portion of the clock cycle, thereby outputting a first plurality of product-output signals, and responsive to said multiplexer selecting the second plurality of shift registers during the second portion of the clock cycle, for multiplying the second portion of the reference-chip-sequence signal by the plurality of input-data samples during the second portion of the clock cycle, thereby outputting a second plurality of product-output signals;

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an adder tree, comprising a plurality of adder gates coupled to said plurality of XOR gates, for summing the first plurality of product-output signals during the first portion of the clock cycle, thereby generating a first sum, and for summing the second plurality of product-output signals during the second portion of the clock cycle thereby generating a second sum;

a memory, coupled to said adder tree, for storing the first sum outputted from said adder tree during the first portion of the clock cycle; and

an adder, coupled to said adder tree and to said memory, for adding the first sum stored in said memory to the second sum from said adder tree.

Cancel claims 2-17 and add the following claims:

~~2~~ ~~18~~. The spread-spectrum-matched filter as set forth in claim 1, further comprising a gate coupled to an input of said plurality of data-shift registers for turning off any section of said spread-spectrum-matched filter responsive to a processing gain input.

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~~19~~. The spread-spectrum-matched filter as set forth in claim 1, further comprising a plurality of AND gates coupled to inputs of said plurality of data-shift registers, respectively, one input of each of the AND gates being used to control enablement of said spread-spectrum-matched filter.

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~~20.~~ The spread-spectrum-matched filter as set forth in claim 1, said plurality of data-shift registers further comprising:

a plurality of in-phase data-shift registers; and

a plurality of quadrature-phase data-shift registers.

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~~21.~~ The spread-spectrum-matched filter as set forth in claim ~~20~~ 4, said plurality of exclusive-OR (XOR) gates further comprising:

a plurality of in-phase XOR gates for multiplying the first portion of the reference-chip-sequence signal by a plurality of in-phase input-data samples during the first portion of the clock cycle; and

a plurality of quadrature-phase XOR gates for multiplying the second portion of the reference-chip-sequence signal by a plurality of quadrature-phase input-data samples during the second portion of the clock cycle.

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~~22.~~ A spread-spectrum-matched filter, for use as part of a spread-spectrum receiver on a received-spread-spectrum signal having a plurality of information bits with the received-spread-spectrum signal generated from spread-spectrum processing each information bit with a chip-sequence signal, comprising:

reference means for storing a plurality of portions of a reference-chip-sequence signal;

control means for generating a clock signal having a clock rate with a clock cycle;

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multiplexer means, coupled to said reference means and responsive to the clock signal, for outputting, sequentially, from said reference means and through said multiplexer means, each portion of the plurality of portions of the reference-chip-sequence signal during a respective portion of the clock cycle;

data-register means, coupled to said spread-spectrum receiver, for shifting a plurality of in-phase input-data samples and a plurality of quadrature-phase input-data samples of the received-spread-spectrum signal at the clock rate;

multiplying means, coupled to said data-register means and through said multiplexer means to said reference means, for multiplying a respective portion of the reference-chip-sequence signal by the plurality of in-phase input-data samples and by the plurality of quadrature-phase input-data samples located in said data-register means during the respective portion of the clock cycle, thereby outputting a respective plurality of product-output signals;

summing means, coupled to said multiplying means, for summing each plurality of product-output signals during the respective portion of the clock cycle, thereby generating a plurality of sums corresponding to the plurality of portions of the reference-chip-sequence signal;

memory means, coupled to said summing means, for storing the plurality of sums; and

adder means, coupled to said summing means and to said memory means, for adding the plurality of sums.

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~~23~~. The spread-spectrum-matched filter as set forth in claim 6 ~~22~~, said reference means further comprising:

first reference means for storing a first portion of a reference-chip-sequence signal; and

second reference means for storing a second portion of the reference-chip-sequence signal;

said multiplexer means, coupled to said first reference means and to said second reference means and responsive to the clock signal, for outputting, from said first reference means, through said multiplexer means, the first portion of the reference-chip-sequence signal during a first portion of the clock cycle, and for outputting, from said second reference means, the second portion of the reference-chip-sequence signal during a second portion of the clock cycle.

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~~24~~. The spread-spectrum-matched filter as set forth in claim 6 ~~22~~, said data-register means comprising:

a plurality of in-phase data-shift registers; and

a plurality of quadrature-phase data-shift registers.

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~~25~~. The spread-spectrum-matched filter as set forth in claim 6 ~~22~~, said multiplying means comprising:

a plurality of in-phase XOR gates for multiplying the first portion of the reference-chip-sequence signal by a plurality of in-phase input-data samples during the first portion of the clock cycle; and

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